REMARKS

The Examiner is thanked for the due consideration given the application. The specification has been amended to add headings and to better refer to the drawings.

Claims 33-63 are pending in the application. The claims have been amended to better set forth the invention.

No new matter is believed to be added to the application by this amendment.

Information Disclosure Statement

The Official Action asserts that U.S. Patent 6,073,085 must be submitted in a new Information Disclosure Statement (IDS) because the "incorrect inventor" was identified in the IDS filed December 8, 2005.

In the IDS filed December 8, 2005, the PTO-1449 form identified U.S. Patent 6,073,085 as being by "KOU ABRAHAM H ET AL". Abraham H. Kou was the second listed inventor on the patent. The first listed inventor on the patent was Robert A. Wiley. It is also noted that the International Search Report listed the inventor of U.S. Patent 6,073,085 as "KOU ABRAHAM H ET AL". From this, the provenance of U.S. Patent 6,073,085 is believed to be clear.

37 CFR §1.98(b)(1) states: "Each U.S. patent listed in an information disclosure statement must he identified by inventor, patent number and issue date." However, there is no

requirement in 37 CFR §1.98(b)(1) that the named inventor must be the first inventor listed on the patent.

37 CFR §1.97(f) states: "If a bona fide attempt is made to comply with §1.98, but part of the required content is inadvertently omitted, additional time may be given to enable full compliance."

For convenience, a supplementary PTO-1449 form is attached to this paper, in which U.S. Patent 6,073,085 is identified by the first named inventor. It is respectfully requested that an initialed PTO-1449 form be made of record in the next Official Action.

The Specification

The Official Action sets forth preferred guidelines for the layout of the specification. The specification has been amended to insert headings.

The Drawings

The drawings have been objected to as showing a reference character not discussed in the specification, i.e., reference numeral 7 in Figures 8-10.

The specification has been amended to refer to numeral 7 in Figures 8-10.

Claim Objections

Claim 60 is objected to as not having a status identifier. In this paper, claim 60 has been given a status identifier appropriate to its current status.

Rejection Under 35 USC §112, Second Paragraph

Claims 33-63 have been rejected under 35 USC §112, second paragraph, as being indefinite. This rejection is respectfully traversed.

The comments set forth in pages 4-7 have been considered, and the claims have been amended in light of these comments. The claims are thus clear, definite and have full antecedent basis.

This rejection is believed to be overcome, and withdrawal thereof is respectfully requested.

Rejections Over OCHS et al.

Claims 33-45, 47, 51, 53-55, and 58-63 have been rejected under 35 USC §102(b) as being anticipated by OCHS et al. (U.S. Patent 5,899,925). Claims 46, 48-50 and 52 have been rejected under 35 USC §103(a) as being unpatentable over OCHS et al. These rejections are respectfully traversed.

The present invention pertains to a medical device having components that can autonomously initiate a self-test routine independently of the operation of the medical device. The present invention is typically illustrated, by way of example, in Figure 3 of the application, which is reproduced below.

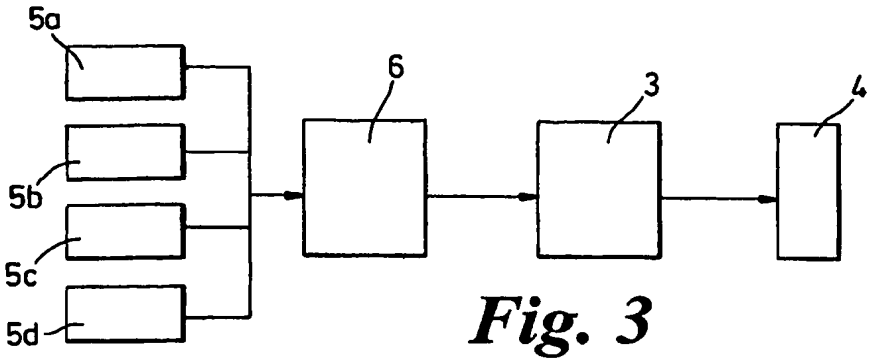


Fig. 3

As shown in Figure 3, data from the individual components 5(a) to 5(d) is fed as an output from test circuits for the individual components, and these are fed to a communication output as a collated signal, which passes to the summator 6. Information from the summator is then fed by a communication link to a processor 3, and the central processing unit in the processor collates the information from the summator with stored memory data concerning the components being tested. A single communication link sends an output to the indicator 4, for example a digital display, to show the status of the combined data from the components 5(a) to 5(d).

Claim 1 of the present invention sets forth multiple components, each of which has a respective self-test means associated therewith adapted to carry out a self-test routine on the associated component. Claim 1 of the present invention additionally sets forth that each of the self-test means is activated independently of operation of the medical device and

not by a signal from a processor associated with the medical device, with results thereof being passed to a common processor.

In comparison, as is discussed in the specification, conventional testing of the various components of a medical device has hitherto been accomplished by a central processor sending out a signal to each component to initiate a self-test. This is problematic as it may cause a critical delay when the machine is powered up to allow for the central processor to instruct each self-test unit to carry out its test, wait for the test results and then analyze them. Also, such testing requires active intervention by the central processor which, in turn, means that the device needs to be fully operational to allow the testing to be carried out.

In contrast, the components in the present invention are able to initiate and perform self-testing autonomously, without the intervention of the central processor, while the remainder of the equipment is in a quiescent mode. This means that the testing can be carried out when the central processor is not on.

OCHS et al. pertain to aperiodic self-testing of a defibrillator. The Official Action refers to Figures 1 and 2 of OCHS et al. Figure 2 of OCHS et al. is reproduced below.

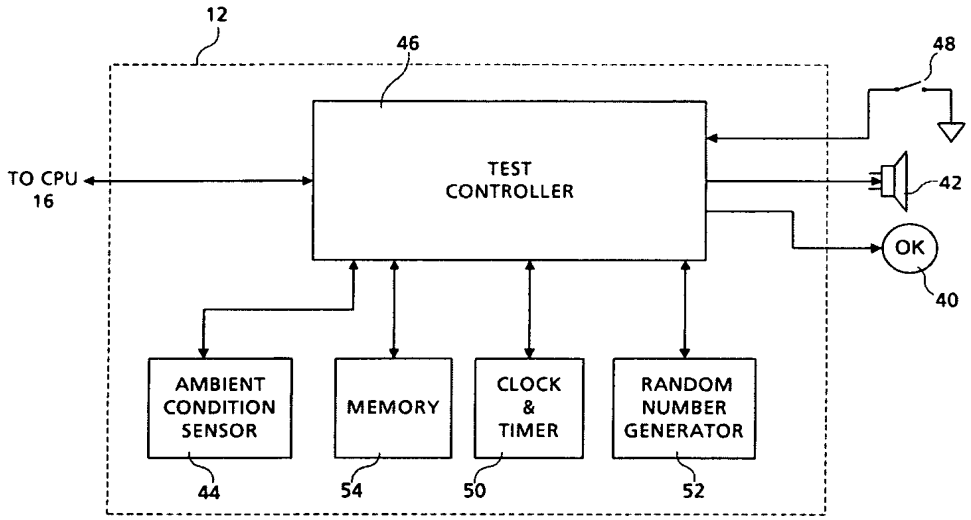


FIG. 2

OCHS et al. discuss a system in which the defibrillator components may have circuitry for testing and communicating component status to the CPU 16 and the system monitor 12. There is no teaching or inference in OCHS et al. of a self-test arrangement in which the test is initiated by independent self-test units. It is clear from column 3, lines 47 to 49 of OCHS et al. that the system monitor is responsible for initiation of the self-testing and so it is clear that all testing is initiated centrally by the monitor 12.

That is, column 3, lines 47-49 of OCHS et al. states: "The system monitor 12 generates test signals at various times and in response to specified events, such as power-on events, to initiate testing of defibrillator functions."

OCHS et al. fail to teach a plurality of components, which carry out a self-test routine and that are activated independently of operation of a medical device and not by a signal from a processor associated with a medical device as expressly required by independent claims.

Nonetheless, the Official Action asserts that OCHS et al. teach a self test routine activated independently of operation of the medical device and not by a signal from a processor associated with the medical device.

Column 3, line 6 to column 4, line 5 of OCHS et al. discuss the various tested defibrillator components may itself contain circuitry for testing and communicating component status to the CPU 16 and system monitor 12. For example, the ECG circuit 24 may include a signal generator for generating test ECO signals to test ECG amplifier and analogue-to-digital converter functions.

However, the signal generator of OCHS et al. generates a test ECG signal and not an activation signal. If the signal generator is to be an activation signal generator, then a second ECG test signal generator would be required to further conduct the test and no such provision exists. OCHS et al. clearly intended the signal generator to simulate an ECG signal similar to that produced by the human heart in order to test the operations of the ECG circuitry. OCHS et al. fail to teach this signal generator being self-activated. On the contrary, OCHS et

al. teach that the activation signals are generated from the centralized system monitor 12.

Also, column 3, lines 54-59 of OCHS et al. discusses that the system monitor 12 applies test signals to the CPU 16, and the CPU controls and gathers information from various tested defibrillator components.

OCHS et al. additionally discuss a high voltage delivery circuit 18 including a test load circuit to which a high voltage pulse is delivered instead of the electrode connector 20 (column 3, lines 23-24). If the assertions in the Official Action were to be applied to OCHS et al., then the high voltage pulse for testing the delivery circuit 18 would equally be the activation signal. Such an arrangement would be dangerous and is clearly not the case. Rather, it is the intention of OCHS et al. that an initiation signal is sent first from system monitor 12 to the test load circuitry of the delivery circuit 18 and only upon receipt of this signal is a self-test conducted and the results relayed back to system monitor 12.

Additionally, the Official Action's position that the system monitor 12 as taught in column 4, lines 14-19 also meets the claimed limitation in that it is "not a centralized processor" like CPU 16, is a mischaracterization of the technology of OCHS et al. The system monitor 12 of OCHS et al. is clearly a centralized processor akin to CPU 16. Its function is undoubtedly the single point of centralized control and

communication to the various independent defibrillator components. This differs from the present invention, where each of the various defibrillator components has their own unique and independent system monitor and are thus "decentralized".

The Official Action asserts that the system monitor 12 of OCHS et al. is activated by its own separately dedicated power supply. However, nothing in OCHS et al. supports such an assumption. The activation of the system monitor 12 in OCHS et al. is governed by timer circuit 50 as taught in column 4 lines 48-53. The system monitor 12 automatically tests defibrillator functions at random or otherwise aperiodic time intervals. The intervals may be determined by the random number generator 52 providing signals for loading the timer circuit 50. See column 2, lines 19-23. The timing circuit produces a timing signal following elapse of a given time interval, and the testing controller receives the timing signal and initiates test procedures in response thereto.

The Official Action further asserts that OCHS et al. teach a summator combining elements of gate array 26, removable memory 30 and system monitor 12.

However, the gate array 26 element of OCHS et al. acts to integrate many of the defibrillator's functions, such as display control, and many instrument control functions (column 3, lines 33-35). The task of the removable memory 30 is not taught by OCHS et al. However, one must assume that it is employed for

storing data used to initiate defibrillator self-test operations in a manner similar to memory 54 (column 4, lines 35-37). The system monitor 12 generates test signals at various times to initiate testing of defibrillator functions (column 3, lines 47-49). None of these elements combine to perform the same function of the summator as defined by the present invention.

Regarding claim 62, the Official Action asserts that OCHS et al. disclose a self test that is aperiodic. However, OCHS et al. fail to teach the structure of the present invention, and any aperiodicity in OCHS et al. is merely coincidental.

Regarding claims 41-45 and 47, the Official Action asserts that OCHS et al. disclose a summator that is a micro-controller, includes a subtractor component, and is part of a main microprocessor. The Official Action additionally asserts that OCHS et al. disclose a signal being a number of pulses as a prime number, and that a self test is triggered by a test carried out by another component.

However, the summator of the present invention is not a test controller and, consequently, it is of no importance whether the summator is a microcontroller, a CPU or otherwise. The summator of the present invention acts only to passively record the results of tests conducted outside of its remit. OCHS et al. thus fail to teach the summator of the present invention.

Further, the passage in column 7, lines 1-2 of OCHS et al. fails to teach a subtractor component. OCHS et al. merely

teach that the selection and order of certain steps (within the procedure of Figures 3 and 4) can be readily modified, and some steps omitted and others added. There is additionally no structure disclosed for identifying self-test results.

Also, the pulses of the claimed invention are merely a way to identify a component. There is no teaching or suggestion in OCHS et al. of a signal containing a number of pulses as a prime number, as is set forth in claims 44 and 45 of the present invention.

Additionally, the test load circuitry in column 3, line 67 of OCHS et al. is a physical resistive load, commonly referred to as a resistor, capable of dissipating the high voltage pulse delivered to it from the high voltage delivery circuit 18 as an alternative to the electrode connector. The load being referenced in column 6, line 37 of OCHS et al. is a common term for the amount of electrical power that is drawn from a line or source, and it is not a physical component.

The Official Action's position that such a load (be it a physical resistive load or a common term) makes up part of a summator thus is misdescriptive both in that this earlier comparative definition was mistaken and also that such a component made up no part of this definition.

Finally, OCHS et al. fail to teach or suggest a self-test triggered by a test having been carried out on another component. OCHS et al. teach adjusting the mean frequency of the

aperiodic testing to provide more frequent testing (column 5, lines 25–27) and in addition, the system monitor 12 generates test signals at various times and in response to specified events, such as power on events, to initiate testing of defibrillator functions (column 3, lines 47–49). OCHS et al. suggest that such specified events could be detected changes in environmental conditions such as temperature or humidity (column 5, lines 47–56) OCHS et al. determine the various conditional parameters by means of a sensor 44 (column 6, lines 23–27). However, OCHS et al. fail to teach a self-test independent of operation of the medical device, as is forth in the independent claims of the present invention.

As a result, OCHS et al. fail to anticipate or render *prima facie* unpatentable the structures and functions set forth in independent claims 33, 36 and 61. Claims depending upon these independent claims are patentable for at least the above reasons.

These rejections are believed to be overcome, and withdrawal thereof is respectfully requested.

Rejection Over POWERS et al.

Claims 33-43, 51, 53-56 and 58-63 have been rejected under 35 USC §102(b) as being anticipated by POWERS et al. (U.S. Patent 5,879,374). This rejection is respectfully traversed.

POWERS et al. pertain to an external defibrillator with automatic self-testing prior to use. The Official Action asserts that POWERS et al. disclose a plurality of components carrying

out a self test routine and activated independently of operation of a medical device and not by a signal from a processor associated with a medical device. The Official Action refers to Figures 3-6 of POWERS et al. Figure 3 of POWERS et al. is reproduced below.

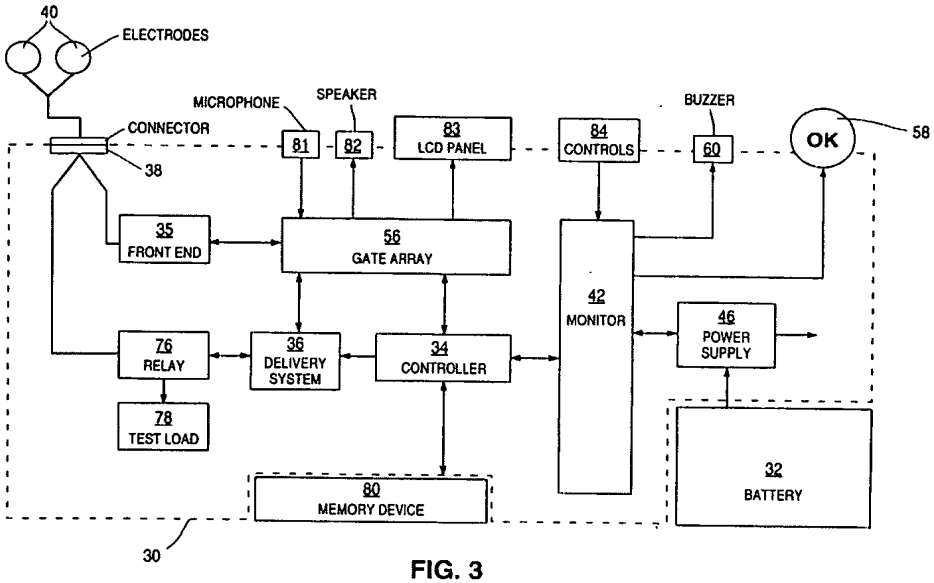


FIG. 3

POWERS et al. fail to teach a plurality of components, which carry out a self-test routine and that are activated independently of operation of a medical device and not by a signal from a processor associated with a medical device as expressly required by independent claims.

The Official Action asserts that the signals through the electrodes 40 that are sent to the system gate array 56, which causes the signal generator 94 to emit a test signal is not an example of two different components (electrodes and relay)

activated independently of operation of a medical device and not be a signal from a processor associated with a medical device.

However, this assertion represents a misinterpretation of the arrangement of POWERS et al. Only when in use on a patient are signals sent to the system gate array 56 ***from*** electrodes 40. Column 4, lines 44-46 of POWERS et al. discusses that an ECG front end system 35 acquires and pre-processes the ***patient*** ECG signals through electrodes 40 and sends the signals to CPU 34 via a system gate array 56. These signals, acquired from the patient, do not result in the system gate array 56 instructing signal generator 94 to emit a test signal, as is asserted in the Official Action. The sole purpose of POWERS et al. is an automatic self test prior to use.

In the defibrillator connector/relay self-test, the initiation of the test is ultimately a consequence of receiving a signal from the system monitor (column 4, lines 63—67, column 5, lines 1-3) the gate array 56 being pre-programmed to perform the functions of the system monitor (column 5, lines 16—18). Upon receipt of this signal, the gate array 56 uses the signal generator 94 as a test signal injector to verify the various ECG front-end elements, wiring to the patient connector 38, and the normally open contacts of the test and isolation relay 76 (column 8, lines 56-60).

The defibrillator has a testing system 24 including a test signal generator 25 of which the purpose of testing system

24 is to test the operational status of the defibrillators components in response to pre-determined events or conditions and/or periodically on a preset schedule (column 3, lines 21-25). It is clear the intention of POWERS et al. is that any test undertaken within the defibrillator is a result of a signal originating from a centralized processor associated with the device, and none of the components are tested independently of operation of the device as expressly required by the claims of the present invention.

The Official Action additionally asserts that POWERS et al. disclose a summator formed from a combination of the gate array 56, memory 3 and system monitor 42, as per column 7, lines 21-35 in combination of indicator elements 83 and LCD 58. However, these disparate components fail to form a summator for the same reasons that the disparate elements of OCHS et al. (discussed above) fail to form a summator.

Regarding claims 51 and 56, the Official Action further asserts that POWERS et al disclose testing a voltage across substantially all of the circuitry (Figure 8 and column 11, lines 8-18), and set parameters to provide an indication of whether one ore more components are functioning as required (column 7, lines 29-30). However, POWERS et al. fail to disclose any such testing means, and column 11, lines 8-18 of this reference instead refer to a protection means commonly known for the prevention of the

effects of excessive voltage in the event of a height than expected patient load resistance.

POWERS et al. thus fail to anticipate a claimed embodiment of the present invention, particularly in regards to independent claims 33, 36 and 61. Claims depending upon these independent claims are patentable for at least the above reasons.

This rejection is believed to be overcome, and withdrawal thereof is respectfully requested.

Conclusion

The prior art of record but not utilized is believed to be non-pertinent to the instant claims.

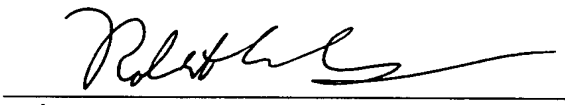
The objections and rejections are believed to have been overcome, obviated or rendered moot, and that no issues remain. The Examiner is accordingly respectfully requested to place the application in condition for allowance and to issue a Notice of Allowability.

The Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any

overpayment to Deposit Account No. 25-0120 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17.

Respectfully submitted,

YOUNG & THOMPSON



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Appendix:

The Appendix includes the following item:

- supplemental PTO-1449 Form